PVP 20

Code: 20CS3301, 20IT3301

II B.Tech - I Semester – Regular Examinations - FEBRUARY 2022

FUNDAMENTALS OF DIGITAL LOGIC DESIGN

(Common for CSE, IT)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

UNIT – I

1. a) Convert the following octal numbers to hexadecimal
   i) 2035 ii) 1762.46 iii) 6054.263 7 M
   b) Show that
   i) $AB + A\bar{B}C + B\bar{C} = AC + B\bar{C}$
   ii) $A\bar{B}\,C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B+C$ 7 M

OR

2. a) Perform the following subtractions in XS-3 code using 9's compliment
   i) 687 – 348 ii) 246 – 592 7 M
   b) Without reducing, convert the following expressions to NAND logic
   i) A+BC+ABC
   ii) (XY+Z) (XY)
   iii) (1+A) (ABC) 7 M

UNIT – II

3. a) Reduce the following expressing using K-map
   i) (A+B) (A+$\bar{B}$+C) (A+$\bar{C}$)
   ii) A(B+$\bar{C}$) (A+$\bar{B}$) (B+C+$\bar{D}$)
   7 M

   b) Reduce the following expression
   $F = \sum m (2,3,6,7,8,10,11,13,14)$
   and implement it using NOR Gates. 7 M

OR

4. a) Realize the XOR function using
   i) AOI logic ii) NAND logic 7 M

   b) Reduce the following expression
   $F = \prod M (2,8,9,10,11,12,14)$ and implement it in universal logic. 7 M

UNIT-III

5. a) Design a 4-bit binary to BCD converter.
   7 M

   b) Implement the logic function using an 8 X 1 Multiplexer.
   $F (A, B, C, D) = \sum m (1,3,4,11,12,13,14,15)$ 7 M

OR

6. a) Give the necessary logical circuit for carry generation in Carry-Look-Ahead adder. 7 M

   b) Design a Full Adder circuit and realize it using two half adders. 7 M

UNIT – IV

7. a) Convert the S-R flip-flop to J-K flip-flop using conversion table and implement the logic diagram. 7 M

   b) Explain the SR flip flop with necessary diagrams. 7 M

OR

8. a) Distinguish between JK flip-flop and Master Slave JK flip-flop. 7 M

   b) Convert the J-K flip-flop to S-R flip-flop using conversion table and implement the logic diagram. 7 M

UNIT – V

9. a) Design a Mod-9 Synchronous counter using T- FF. 7 M

   b) With neat diagram explain the 4-bit Serial-in, Parallel-out shift Register. 7 M

OR

10. a) Design an up/down counter using D FF's to count 0,3,2,6,4,0 …. 7 M

    b) What is universal shift register and explain with neat diagram. 7 M